REMARKS/ARGUMENTS

Claims 1-19 are pending in the application. Claims 1, 7, and 11 were amended.

The specification, abstract, and claims 1 and 7 were objected to. Claim 11 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claim 7 was rejected under 35 U.S.C. §112, second paragraph, as having insufficient antecedent basis for one of its elements. Claims 1, 5, 7, 14, and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by Swoboda et al., U.S. Patent No. 6,643,803 (hereinafter "Swoboda"). Claims 2, 8, and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Sato, U.S. Patent No. 5,903,768 (hereinafter "Sato"). Claims 3-4, 6, 9-11, 16-17, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam et al., U.S. Patent No. 6,285,974 (hereinafter "Mandyam"). Claims 12-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam in further view of Hennessy and Patterson, Computer Organization and Design, 2nd Edition, 1998 (hereinafter "Hennessy").

Objections to the Abstract, Specification, and Claims

The specification, abstract, and claims 1 and 7 were objected to. The specification, abstract, and claims 1 and 7 have each been amended to overcome these objections. On page 8, line 13, the phrase "program start to program start" is correct.

Claim Rejections Under 35 U.S.C. §112

Claim 11 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claim 11 has been amended to overcome this objection.

Claim 7 was rejected under 35 U.S.C. §112, second paragraph, as having insufficient antecedent basis for one of its elements. Claim 7 has been amended to overcome this objection.

Claim Rejections Under 35 U.S.C. §102(e)

Claims 1, 5, 7, 14, and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by Swoboda. Swoboda generally discloses emulation and debug circuitry that can be incorporated into a variety of digital systems (*See* Abstract).

Swoboda does not disclose an execution stage of a processor to execute a neutral instruction to ascertain an architectural state value for the processor, as recited by claims 1, 7, and 14. The Office Action cites the Abstract of Swoboda, which states:

> While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to cause processor resources to be read or written on behalf of the emulation circuitry.

(*See* Swoboda, Abstract).

The instruction in question causes the processor to be read, but Swoboda does not state that the instruction is a read instruction, or that the processor executes the read. The specification of Swoboda states:

> The register is in the generic component while the placement of the register in the memory map and the logic needed to read the register is in the wrapper. Models for the generic component can be easily ported from design to design, modulated to optimize bus widths when required.

(*See* Swoboda, Col. 8, Lines 52-55).

> Debug software can use two mechanisms to get to system resources. This instruction directly supports one of them, the MU option. The memory unit (MU) provides register set (an address register and write data register) that debug software loads for each access. The address register doubles as the read data input register. Once the read is initiated, the address is no longer needed so this does not present a problem. The address register is loaded through the write data register. Debug software provides the address for each read access and initiates the read access with a single instruction scan. It must end in the

IDLE state, passing directly from the Update_IR to the IDLE state to load the address.

A second read option, indirectly supported by this instruction, requires the address comparison unit (ACU) to supplement the MU registers with auto incrementing address generation. Debug software allocates the ACU to breakpoints, PSA generation, timing and benchmarking features, and DMA address generation. During data logging the application uses the ACU DMA facilities while production tests use the DMA facilities to expedite test down loads. Because of the multifunction aspects of the ACU, it is not generally used for low bandwidth transfers.

(*See* Swoboda, Col. 13, Lines 45-67).

In other words, the read is performed by the debug architecture, and not by the processor execution stage. Furthermore, Swoboda does not indicate that the state is not altered by these instructions. Therefore, Swoboda does not disclose the execution stage of a processor executing a neutral instruction to ascertain an architectural state value for the processor. Applicants respectfully submit, therefore, that elements of claim 1, 7, and 14 are neither shown nor suggested by the cited reference. Claims 5 and 18 depend from claims 1 and 14, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 1, 5, 7, 14, and 18 under 35 U.S.C. §102(e) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 2, 8, and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Sato. Sato discloses a pipelined microprocessor capable of avoiding pipeline stalls (*See* Abstract). One of the disclosed methods is by inserting a NOP operation into the pipeline (*See* Sota, Col. 2, Lines 4-14).

Neither Swoboda, Sato, nor any combination thereof discloses the execution stage of a processor executing a neutral instruction to ascertain an architectural state value for the processor, as recited by claims 1, 7, and 14.

Applicants respectfully submit, therefore, that elements of claims 1, 7, and 14 are neither shown nor suggested by the cited references. Claims 2, 8, and 15 depend from claims 1, 7, and 14, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 2, 8, and 15 under 35 U.S.C. §103(a) is respectfully requested.

Claims 3-4, 6, 9-11, 16-17, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam. Mandyam discloses detecting architectural violations in a multiprocessor computer system using a random test generator.

Neither Swoboda, Mandyam, nor any combination thereof discloses the execution stage of a processor executing a neutral instruction to ascertain an architectural state value for the processor, as recited by claims 1, 7, and 14.

Applicants respectfully submit, therefore, that elements of claims 1, 7, and 14 are neither shown nor suggested by the cited references. Claims 3-4, 6, 9-11, 16-17, and 19 depend from claims 1, 7, and 14, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 3-4, 6, 9-11, 16-17, and 19 under 35 U.S.C. §103(a) is respectfully requested.

Claims 12-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam in further view of Hennessy. Hennessy is a computer textbook that discloses AND and OR operations.

Neither Swoboda, Mandyam, Hennessy, nor any combination thereof discloses the execution stage of a processor executing a neutral instruction to ascertain an architectural state value for the processor, as recited by claim 7.

Applicants respectfully submit, therefore, that elements of claim 7 are neither shown nor suggested by the cited references. Claims 12-13 depend from claim 7. Accordingly

reconsideration and withdrawal of the rejection of claims 12-13 under 35 U.S.C. §103(a) is respectfully requested.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

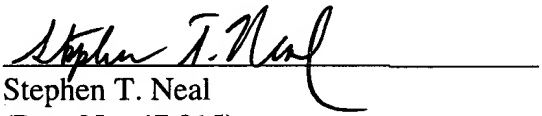
The Commissioner is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON

Dated: June 17, 2004

By: 
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